**CLAIMS:**

What is claimed is:

1. A semidigital delay-locked loop circuit comprising:

a controllable delay element having a clock input and a phase input, and a clock signal output, wherein signals on the clock signal output have a changing phase controlled by phase data received at the phase input;

a phase detector, a first input, a second input, an up output, a down output, and a data output, wherein data is received at the first input , the second input is connected to the clock signal output, and wherein the phase detector generates up signals through the up output and down signals through the down output in response to data received at the first input; and

an analog based finite state machine having an up input connected to the up output, a down input connected to the down output, and phase output connected to the phase input of the controllable delay element, wherein the analog based finite state machine generates the phase data in response to up signals and down signals received from the phase detector.

2. The semidigital delay-locked loop circuit of claim 1, wherein the phase data includes data for phase interpolation and data for phase selection.

3. The semidigital delay-locked loop circuit of claim 1, wherein the analog based finite state machine comprises:

a charge pump; and

a logic unit.

4. The semidigital delay-locked loop circuit of claim 1, wherein the logic unit comprises:

an analog to digital converter, wherein the analog to digital converter generates a logic signal in response to a voltage signal from charge pump;

a level detector, wherein the level detector generates a first signal and a second signal in response to voltage level changes in the voltage signal from the charge pump; and

a state machine, wherein the state machine generates a phase logic signal in response to first signal and the second signal.

5. The semidigital delay-locked loop circuit of claim 4, wherein the analog to digital converter has a 3 bit output.

6. The semidigital delay-locked loop circuit of claim 4, wherein the state machine has a state that changes states in response to the first signal and the second signal and the logic signal is generated in response to the state of the state of the state machine.

7. The semidigital delay-locked loop circuit of claim 6, wherein the state machine has four states.

8. The semidigital delay-locked loop circuit of claim 7, wherein the state machine generates a "00" signal in a first state, a "01" signal in a second state, a "10" signal in a third state, and a "11" signal in a fourth state.

9. The semidigital delay-locked loop circuit of claim 1 further comprising:

a polyphase filter having an input for receiving the clock signal and an output connected to the clock input of the phase rotator, wherein the polyphase filter generates

four clock signals in which each clock signal has a different phase.

10. The semidigital delay-locked loop circuit, wherein the polyphase filter includes a plurality of capacitors and a plurality of resistors.

11. The semidigital delay-locked loop circuit 9 further comprising:

a clock circuit having an input and an output, wherein the input of the clock circuit is connected to a clock signal and wherein the output of the clock circuit is connected to the input of the polyphase filter.

12. The semidigital delay-locked loop circuit of claim 11, wherein the clock circuit is a phase locked-loop circuit.

13. The semidigital delay-locked loop circuit of claim 11, wherein the clock circuit is a delay locked-loop circuit.

14. The semidigital delay-locked loop circuit of claim 1, wherein the phase detector has tristate operation.

15. The semidigital delay-locked loop circuit of claim 1, wherein the controllable delay element is a phase rotator.

16. The semidigital delay-locked loop circuit of claim 1, wherein the analog to digital converter is a 1.5 bit analog to digital converter.